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(System-on-Chip). This Has Made Verification The Most Critical Bottleneck In The Chip Design Flow. Roughly 70 To 80 Percent Of The Design Cycle Is Spent In Functional Verification. [1]System Verilog Is A Special Hardware Verification Language To Be Used In Function Verification. It Provides The High-level Data Structures Available 7th, 2024

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UVM Is An Open Source Veri Cation Standard. The UVM Package Is Maintained By The Accellera UVM Working Group [9]. It Is A Library Built Upon The SystemVerilog Language [13]. It Provides Base Classes Such As Uvm Component To Construct The Structure Of The Testbench, Uvm Object To Serve As Data Structures Used In The 1th, 2024

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