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Used With Binary Logic Elements Where The Logic State 1 (TRUE) Is Converted To A
Logic State 0 (FALSE) Or Vice Versa [IEC 60617-12, IEC 61082-2] 3.20 Logic
Inversion Condition Mainly Used With Binary Logic Elements Where A Higher
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See The Data Sheet For The Pic 16F84A For All Instructions. Remember That A 10%
Duty Cycle Wave Means That The Output Is Positive 10% Of The Time. Next Lets Do
A Few Modifications To Our first Program Than Interacts With The Real World. The
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