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Sep 25, 2009 · Toolchain. For More Information About The SMIPS Toolchain Consult Tutorial 3: Build, Run, And Write SMIPS Programs. VCS Takes A Set Of Verilog files As Input And Produces A Simulator. When You Execute The Simulator You Need Some Way To Observe Your Design So That You Can Measure Its Performance And Verify That It Is Working Correctly. Mar 1th, 2024

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- Testbench Just Sends 32 Bytes To Serializer/deserializer - Each Time A New Byte Comes Out Of The Deserializer, It Is Printed To Screen. • Synopsys Script File Ser.script For Testing If Verilog Code Is Synthesizeable. - Your Synthesized Gate Level Code Must Produce Same Result As RTL Apr 7th, 2024

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- “FPGA Prototyping By VHDL Examples –Xilinx Spartan-3 Version, By Pong P. Chu, 2008, Wiley
- “RTL Hardware Design Using VHDL –Coding For Efficiency, Portability, And Scalability” By Pong P. Chu, 2008, Wiley.
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