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Saturated Baking Soda (sodium Hydrogen Carbonate),
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Solution, (pH = 9) 4-5 Drops Phenolphthalein
Indicator 10 ML Saturated Magnesium Chloride, MgCl₂(aq)
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[12]. However, It Is Admitted That This Design, By Its
Nature, Is Still Sensitive To Single-node Upsets During
The Hold State. As Illustrated In Fig. 1(b), After The
Internal Node B Holding Logic 0 Is Hit, The Logic States
Of This Latch Structure Would Flip. Therefore, A

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Single Power Supply Single Buffer GATE CMOS ... Able
To Support 1.8-V, 2.5-V, 3.3-V, And 5-V CMOS Levels.
The Input Is Designed With A Lower Threshold Circuit
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